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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/518,608 | 12/23/2004 | Salvatore Pappalardo | 02-CT-104/DP | 9027 |

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HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

| EXAMINER | |
|---|---|
| CARTER III, ROBERT E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2629 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 04/22/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentcolorado@hhlaw.com

| **Advisory Action Before the Filing of an Appeal Brief** | **Application No.** 10/518,608 | **Applicant(s)** PAPPALARDO ET AL. | |
|---|---|---|---|
| | **Examiner** ROBERT E. CARTER III | **Art Unit** 2629 | |

***--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

THE REPLY FILED 06 April 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-10*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments are not persuasive. Applicant argues that the Examiner improperly characterized Zukowski's field of endeavor. However, the cascaded multiplexers of Zukowski that the examiner relied upon are a well known structure used in may areas of electronics. Furthermore, there are no unique or inventive features to the cascaded mulitplexer stucture of Zukowski, which is why the Examiner argued it was a simple substitution of one known structure for the other. Therefore the Examiner's characterizations of Zukowski's field of endeavor as "logic controled selection circuits" is valid. Applicant further argues that the logical operation of the claimed inverter is not identical to the 2-1 multiplexer of Zukowski. Applicant supports this argument by comparing a logic table for a logic inverter to a logic table for a 2-1 multiplexer. In making this argument Applicant is improperly charaterizing the claimed inverter as a logic inverter. This issue was previously addressed after the claims were previously amended to claim a "logic inverter" which the Examiner rejected as not being supported by the disclosure. Indeed the reason this language is not supported by the disclosure is that the two transistor inverter of the instant application does not have the same logical operation as a logic inverter. Regardless of Applicant's insistance the contrary, the act of applying different voltages and different timings to the "power terminals" of the inverter turns the power terminals into signal inputs because whatever signal is applied to the selected power terminal is what is passed to the output. As described in Applicant's arguments A logic inver has one input that can only take logic highs or lows (1s or 0s) as inputs, one output that outputs the opposite logic state of the input (i.e. a 1 if the input is 0 or a 0 if the input is 1), and two power terminals which are designed to be permantly tied to constant power and ground voltages. By contrast the two transistor inverter of the instant application has one one logical input (gates of transistors T11 and T12) that takes a 0 (VSS) or a 1 (VLCD), two signal inputs (1$^{st}$ and 2$^{nd}$ "power terminals") which accept any signal applied to them (within the electrical breakdown limits of the transistors T11 and T12), and one output terminal (OUT) which will simply output whatever signal is applied to the slelected signal input (1st and 2nd "power terminals"). One can choose to limit the voltages applied to the signal input (1st and 2nd "power terminals") to VDD or VSS as suggested by Applicant, but the invention intentionaly applies other voltages, thereby making 1st and 2nd "power terminals" signal inputs. Like the two transistor inverter of the instant application, a 2-1 multiplexer has a logical input terminal (select input) that takes logic highs or lows (0s or 1s), two signal input terminals that (inputs A and B in Applicant's table) that can accept any signal input applied to it (within the muliplexer's electrical breakdown limits), and one output terminal which will simply output whatever signal is applied to the slelected non-logic input (either 21 or 22). Therefore, just like the two transistor inverter of the instant application, the 2-1 mulitplexer simply selects one of two inputs and passes the signal at that input to the output. Applicant also argues that a 2-1 multiplexer is a six terminal device with the two extra terminals being a power and ground terminal. However, while it is true that a multiplexer has a power and ground terminal, these terminals do not in any way change the operational characteristics of the device (unlike the 1$^{st}$ and 2$^{nd}$ power terminals of Applicant's two transistor inverter). Furthermore, almost all basic logic circuits have power and ground terminals. In fact they are so ubiquitous and well known in the art that they are left out of most circuit drawings and descriptions. Applicant's own disclosure includes low voltage logic circuitry 11, level-shifter 12, and a logic inverter between them, all of which also require power and ground terminals, even though they are not shown or described in the disclosure. However the Examiner has not issued an objection or rejection regarding these missing power and ground terminals because their presence is well understood to one of ordinary skill in the art. Therefore, when counting the number of terminals of a logic device, it is common practice to exclude the power and ground terminals (when they are NOT used for signal inputs) just Applicant has done in their own disclosure. Lastly, because they have the same logical operation, in the Final Rejection the Examiner replaces the cascaded multiplexer structure with four terminal two-transistor inverters thereby eliminating the extra power and ground connections of the cascaded multiplexers. For the reasons outlined above, Applicant's arguments are not persuasive and therefore Applicant's request for reconsideration does not place the application in condition for allowance.